Application No.: 09/008,497 Docket No.: 21987-00033-US

REMARKS

Bearing in mind the comments in the Official Action and the amendments and remarks presented herein, the application is believed to be in condition for allowance. An early indication of the same would be appreciated.

Claims 1-9, 21-32, and 34-39 remain pending in this application. Claims 1, 21, 28, 31, 34, 38, and 39 are independent. Independent claims 1, 21, 28, 31, 34, 38, and 39 have been amended, and no claims have been added or canceled by this Amendment. Claim 40 was previously renumbered as claim 39, due to an original numbering error.

Unpatenability Rejections over Chiu OR Matthews

Withdrawal of the rejection of claims 1-9 and 21-40 under 35 U.S.C. §103(a) as being unpatentable over Chiu (US 4,994,402) OR Matthews (US 5,134,083) is requested.

At the outset, Applicant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, ***the prior art reference must teach or suggest all the claim limitations.***[1] Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.[2]

A Prima Facie Case of Unpatentability Has Not Been Established

As a preliminary matter, the undersigned notes that the alternative §103 rejections over Chiu ***OR*** Matthews appears not to be in accordance with the MPEP, nor in line with the USPTO's goal of compact prosecution.

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[1] *See* MPEP §2143.
[2] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.

The presentation of the statement of the rejections appears to invoke language customarily associated with anticipation rejections under 35 U.S.C. §102, and not unpatentability rejections under 35 U.S.C. §103(a).

As indicated above, case law mandates that a *prima facie* case of unpatentability can only be established if there is some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, ***to modify the reference or to combine reference teachings.***

There is no indication in the Official Action of any need to modify or combine any aspect of either Chiu ***OR*** Matthews, and there is no statement provided by the Examiner regarding any claimed limitation which is asserted as not being explicitly present in either reference, such that modification would be required.

Further, the Examiner's statement and purpose is unclear on page 5 of the Official Action which notes that "Chiu and Matthews may have additional steps in their process, however the instant claims include the term 'comprising' that does not exclude additional steps and further current case law states: As a matter of fact selecton of any order of performing process steps is prima facie obvious in the absence of new or unexpected results..."

The fact that the transition term "comprising" is used in the instant claims reflects the fact that applicant's invention is not limited to the claimed limitations. Whether or not Chiu or Matthews may have additional steps is irrelevant to the claimed invention.

Applicant notes that the case incorrectly cited by the Examiner (as *In re Burhaus* on page 5 of the Official Action is actually *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946), cited in MPEP §2144.04. This case stands for the proposition that the selection of a different order of performing process steps is *prima facie* obvious without a showing of new or unexpected results.

However, Applicant has yet not specifically claimed any required order of the steps, thus raising a question of the purpose of this case citation by the Examiner, and its bearing on establishment of a *prima facie* case of unpatentability.

Therefore, Applicants submit that the Examiner has failed to meet his threshold burden in establishing a *prima facie* case of unpatentability of the pending claims. Withdrawal of the unpatentability rejections is requested.

Chiu Teaches Away from at Least One Aspect of Applicant's Claimed Invention

An essential evidentiary component of an obviousness rejection is a teaching or suggestion or motivation to combine the prior art references.[3] Combining prior art references without evidence of a suggestion, teaching or motivation simply takes the inventors' disclosure as a blueprint for piecing together the prior art to defeat patentability – the essence of hindsight.[4]

Chiu teaches away from at least one aspect of Applicant's disclosed and claimed invention, by stating unequivocally that hole alignment is not critical.

In particular, Chiu teaches that "no ill effects are suffered if one of the holes is wider than the pad which lies beneath it or slightly misaligned with respect thereto." (See Chiu at col. 7, lines 50-55). This teaching is directly contrary to at least one objective of Applicant's disclosed and variously claimed invention, i.e, to ensure that the narrow contact hole does not overlap an active region of the device.

For example, independent claim 1, as amended, recites a method for manufacturing a semiconductor device which includes, among other features, "...selectively etching away said second conductive film...so as to process said second conductive film into a pattern in which said second conductive film is separated on said second insulating film by an opening between the second side walls smaller than the minimum processing size achievable with the conventional lithographic process technique, and...***ensuring that the opening between the second side walls does not overlap either of the first sidewall insulating films or either of the source and drain***."

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[3] *C.R. Bard, Inc. v. M3 Systems, Inc.*, 48 USPQ2d 1225 (Fed. Cir. 1998)
[4] *Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed. Cir. 1985)

It is impermissible within the framework of 35 U.S.C. §103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one skilled in the art.[5] Further in this regard, As the Court of Customs and Patent Appeals, predecessor to the Federal Circuit, has held:

> All relevant teachings of cited references must be considered in determining what they fairly teach to one having ordinary skill in the art. The relevant portions of a reference include not only those teachings which would suggest particular aspects of an invention to one having ordinary skill in the art, but also those teachings which would lead such a person away from the claimed invention.[6]

Thus, Applicant submits that a person having skill in the art would not be motivated to rely upon the teachings of Chiu to solve the technical problem addressed by Applicant's disclosed and claimed invention. Therefore, Chiu is not properly combinable with any other reference for the purposes of rendering obvious Applicant's recited invention.

Neither Chiu nor Matthews Acknowledge the Technical Problems Solved

"There are three possible sources for a motivation to combine references: ***the nature of the problem to be solved***, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art."[7] Further with regard to the level of skill of practitioners in the art, there is nothing in the statutes or the case law which makes "that which is within the capabilities of one skilled in the art" synonymous with obviousness.[8] The level of skill in the art cannot be relied upon to provide the suggestion to combine references.[9]

Applicant's disclosed and claimed invention is directed to a method for manufacturing a semiconductor device which has a buried conductive layer connected, in one embodiment, to a source or drain of a MOS transistor through a contact hole having dimensions smaller than that

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[5] *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 230 USPQ 416 (Fed. Cir. 1986).
[6] *In re Mercier*, 185 USPQ 774, 778 (CCPA 1975).
[7] *See* MPEP §2143.01, citing *In re Rouffet*, 149 F.3d, 1350, 1357, 47 USPQ2d 1453, 1457-8 (Fed. Cir. 1998).
[8] *Ex parte Gerlach and Woerner*, 212 USPQ 471 (PTO Bd. App. 1980).

achievable solely by reliance upon available photolithographic processing limits. Further, in view of the sub-photolithographic feature sizes achievable by the recited method, the method of Applicant's invention is designed so as to ensure that the contact hole avoids undesirable and detrimental alignment with an associated sidewall below the contact hole, e.g., sidewalls on a gate structure, and instead generally aligns with a central portion of the device element.

One technical problem solved by Applicant's recited invention is to prevent damage to the silicon substrate due to exposure resulting from the undesirable alignment of the contact hole with the underlying sidewall below the contact hole. Prevention of damage to the underlying substrate, for example, is accomplished by ensuring that the contact hole is, in one embodiment, narrower than an underlying gate length, and is sufficiently centered above the gate structure so as to avoid registration or overlap with any associated sidewall underneath the contact hole.

Chiu is directed to a method of conventional fabrication of a coplanar, self-aligned contact structure in a semiconductor device. Chiu is not directed to provision of feature sizes or holes having dimensions smaller than that achievable by standard photolithographic techniques. In fact, Chiu does not teach or suggest a solution, and does not even acknowledge the technical problems associated with manufacture of semiconductor devices having sub-photolithographic feature sizes, as in Applicant's disclosed and claimed invention.

Matthews is directed to processes for simultaneously fabricating CMOS and bipolar transistors (i.e., "BiCMOS" devices) in the same semiconductor device. Matthews, similar to Chiu, does not acknowledge the technical problem solved by Applicant's disclosed and claimed invention relating to provision of sub-photolithographic feature sizes in a semiconductor device.

Therefore, Applicants submit that a person of ordinary skill in the art would not be motivated to combine or modify either of Chiu or Matthews, such that the unpatentability of the pending claims should be withdrawn.

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[9] *See* MPEP §2143.01, citing *Al-Site Corp. v. VSI Int'l Inc.*, 50 USPQ2d 1161 (Fed. Cir. 1999).

Contrary to the Examiner, Sub-Photolithograpic Features are not Taught by Chiu or Matthews

The Examiner appears to have confused disclosure of "dimensions in the submicron range" (Chiu, col. 2, lines 10-20) and "sub-micron resolutions" (Matthews, col. 1, lines 42-47) with Applicant's disclosed and variously claimed features which are smaller than those achievable by conventional photolithographic techniques.

Applicants submit that the Examiner's assertions regarding submicron dimensions and resolutions are not on point, and are irrelevant to the gist of the disclosed and claimed invention, which relates to ***sub-photolithographic*** features and dimensions, i.e., dimensions which are less than dimensions conventionally achievable by standard photolithograpic techniques. Applicants submit that there is a recognized fundamental conceptual difference between sub-lithographic dimensions (dimensions achievable by conventional photolithographic techniques), and submicron dimensions or resolutions. Submicron size does not equate to sub-photolithographic features or features smaller than those conventionally achievable by photolithograpic techniques.

Neither Chiu nor Matthews Teaches or Suggests all the Claimed Limitations

Neither Chiu nor Matthews teaches or suggests a method for manufacturing a semiconductor device wherein the method includes, among other features, "...selectively etching away said second conductive film with the patterns of said first and second mask layers as a mask so as to process said second conductive film into a pattern in which said second conductive film is separated on said second insulating film by an opening between the second side walls ***smaller than the minimum processing size achievable with the conventional lithographic process technique***...wherein said buried conductive layer includes said second conductive film extending over the gate electrode of the MOS transistor; and ***ensuring that the opening between the second side walls does not overlap either of the first sidewall insulating films or either of the source and drain***", as recited in independent claim 1, as amended (emphasis added).

Neither Chiu nor Matthews teaches or suggests a method of forming a semiconductor device using a lithographic process having a predetermined minimum processing feature size

which includes, among other features, "...patterning the first mask layer to form a slit dividing the first mask layer...***having a width equal in size to the minimum processing feature size*** and having slit side walls...forming a second mask layer on the slit sidewalls, thereby reducing the width of the slit; etching the conductive layer...to separate the conductive layer into at least two conductive layer portions...***separated by a distance which is less than the minimum processing feature size***; and ***ensuring that an area separating the at least two conductive layer portions does not overlap the slit side walls***", as recited in independent claim 21, as amended (emphasis added).

Neither Chiu nor Matthews teaches or suggests a method of forming a semiconductor device which includes, among other features, "...performing conventional photolithography to form a slit in a part of the first mask layer overlying the gate structure...etching the conductive layer using the first and second mask layers as a mask...patterning the conductive layer into at least two portions ***separated by a distance which is less than a minimum processing size achievable by the conventional photolithography***; and ***ensuring that an area between the separated at least two portions does not overlap either of the side faces of the first mask layer in the slit***", as recited in independent claim 28, as amended (emphasis added).

Neither Chiu nor Matthews teaches or suggests a method of manufacturing a semiconductor device, which includes, among other features, "...patterning the first layer to have holes with sidewalls separated by a width equal to a minimum feature size achievable by a conventional lithographic process...***forming a second layer on the sidewalls so as to reduce the width of the holes to be less than the minimum feature size***; patterning a conductive layer beneath the first and second layers using the holes ***to form openings in the conductive layer that are smaller in size than the minimum feature size***; and ***ensuring that the holes having the width less than the minimum feature size do not overlap any diffusion region of the semiconductor device***", as recited in independent claim 31, as amended (emphasis added).

Neither Chiu nor Matthews teaches or suggests a method of forming a semiconductor device which includes, among other features, "...forming a gate electrode overlying the substrate between the source and drain regions, ***the gate electrode having a width no larger than a***

minimum processing size available with a conventional photolithographic process...forming a contact hole in the first layer in an area above the gate electrode, ***the contact hole having a width smaller than the minimum processing size of the conventional photolithographic process***; and ***ensuring that the contact hole does not overlap either of the source and drain regions***", as recited in independent claim 34, as amended (emphasis added).

Neither Chiu nor Matthews teaches or suggests a method of forming a semiconductor device which includes, among other features, "...forming a structure having a first width on a substrate, ***said first width being a minimum feature size achievable by a conventional lithograpic process***...forming slit in the first layer located over the structure, the slit having sidewall spacers separated by a second width, ***wherein the second width is smaller than the minimum feature size achievable with a lithographic process used for making such device***; and ***ensuring that the slit does not overlap an active region of the semiconductor device***", as recited in independent claim 38, as amended (emphasis added).

Finally, neither Chiu nor Matthews teaches or suggests a method of forming a semiconductor device which includes, among other features, "...defining an active area in a substrate with isolation structures, ***the isolation structures each having a width no larger than a minimum processing size available with a conventional photolithographic process...forming a contact hole in the first layer in an area above the isolation structure...having a width smaller than the minimum processing size of the conventional photolithographic process***; and ***ensuring that the contact hole does not overlap the active area in the substrate***", as recited in independent claim 39, as amended (emphasis added).

Therefore, since the applied art, either alone or in combination, does not teach or suggest all the claimed limitations of independent claims 1, 21, 28, 31, 34, 38, and 39, withdrawal of the rejections and allowance of these claims are requested.

Further, as dependent claims 2-9, 22-27, 29, 30, 32, and 35-37 variously and ultimately depend from allowable independent claims 1, 21, 28, 31, 34, 38, and 39, reconsideration and allowance of the dependent claims are also requested.

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In view of the above, each of the presently pending claims Claims 1-9, 21-32, and 34-39 in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

In the event the Examiner believes that an interview would serve to advance prosecution of this application, the undersigned attorney is available at the telephone number indicated below.

For any fee that is due, including fees for extensions of time, please charge CBLH Deposit Account No. 22-0185, under Order No. 21987-00033-US from which the undersigned is authorized to draw.

Respectfully submitted,

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